Amendments to Claims:

This listing of claims will replace all prior versions and listings of claims in the instant application:

Listing of Claims:

1. (Amended) A method of forming an embedded component in a substrate assembly, comprising the steps of:

applying a first conductive layer on a first carrier;

applying a first adhesive layer on the first conductive layer;

placing a pre-processed substrate on the first adhesive layer, wherein the pre-processed substrate includes at least a via;

placing the embedded component in the via, wherein the embedded component includes at least two conductive terminations;

applying a second adhesive layer on at least portions of the pre-processed substrate and above at least portions of the embedded component;

applying a second conductive layer on the second adhesive layer;

placing a second carrier on the second conductive layer; and

biasing the first and second carriers towards each other to create the substrate assembly having the embedded component between the first and second conductive layers such that adhesive from the first adhesive layer and the second adhesive layer flows into the via around the embedded component.

2. (Original) The method of claim 1, wherein the method further comprises the step of:

removing at least one among the first carrier and the second carrier;

forming an opening through at least one pair of layers among a first pair formed from the first conductive layer and the first adhesive layer and a second pair formed from the second conductive layer and the second adhesive layer to expose at least a conductive surface of the embedded component; and

forming an interconnection between the conductive surface of the embedded component and at least one among the first conductive layer and the second conductive layer having the opening.

3. (Original) The method of claim 2, wherein the method further comprises the step of creating a conductive pattern on at least one among the first conductive layer and the second conductive layer.

4. (Original) The method of claim 1, wherein the step of applying the first conductive layer on the first carrier comprises the step of applying a copper sheet on a metallic plate serving as the first carrier.

5. (Original) The method of claim 1, wherein the step of applying the first adhesive layer comprises applying at least one among a first epoxy resin coat, a first thermosetting organic material layer, a first PTFE layer, a first thermoforming organic material layer, a first fiberglass reinforced prepreg layer, and a first thermal plastic dielectric layer over the first conductive layer.

6. (Original) The method of claim 1, wherein the step of placing the embedded component comprises the step of placing the embedded component in a vertical orientation within the via.

7. (Original) The method of claim 1, wherein the step of placing the embedded component comprises the step of dropping the embedded component into the via using a pick and place machine and the method further comprising the step of inspecting the via for the presence of the embedded component.

8. (Original) The method of claim 1, wherein the step of applying the second adhesive layer comprises applying at least one among a second epoxy resin coat, a second thermosetting organic material layer, a second PTFE layer, a second thermoforming organic material layer, a second fiberglass reinforced prepreg layer, and a second thermal plastic dielectric layer over at least portions of the pre-processed substrate and above at least portions of the embedded component and the step of applying the second conductive layer comprises the step of applying a second copper sheet on the second adhesive layer.

9. (Original) The method of claim 2, wherein the step of forming an opening comprises the step of at least one among plasma etching, chemical etching, YAG laser drilling, CO_2 laser drilling, and photo imaging.

10. (Original) The method of claim 3, wherein the step of creating the conductive pattern comprises at least one among the steps of plating, applying photolithography, and etching.

11. (Original) The method of claim 1, wherein the step of biasing the first and second carriers further comprises the step of curing the substrate assembly in a vacuum lamination press such that adhesive from the first adhesive layer and the second adhesive layer flows into the via around the embedded component.

12. (Original) The method of claim 11, wherein the embedded component becomes integrated in the substrate assembly and remains locked in place and aligned within the via.

13. (Amended) A substrate assembly having at least one embedded component in a via of a substrate core, comprising:

a first adhesive layer on a first conductive layer, wherein the first adhesive layer couples the first conductive layer to a bottom surface of the substrate core;

an embedded component in the via, wherein the embedded component includes at least two conductive terminations;

a second adhesive layer on at least portions of a top surface of the substrate core and above at least portions of the embedded component, wherein ~~at least one among~~ both the first adhesive layer and the second adhesive layer at least partially fill[s] the via; and

a second conductive layer on the second adhesive layer.

14. (Original) The substrate assembly of claim 13, wherein the substrate assembly further comprises an interconnection between a conductive surface of the embedded component and at least one among the first conductive layer and the second conductive layer.

15. (Original) The substrate assembly of claim 14, wherein the interconnection is formed through an opening that at least temporarily exposes at least a conductive surface of the embedded component and wherein the opening is through at least one pair of layers among a first pair formed from the first conductive layer and the first adhesive layer and a second pair formed from the second conductive layer and the second adhesive layer.

16. (Original) The substrate assembly of claim 13, wherein the substrate assembly further comprises a first interconnection between a first conductive termination of the embedded component and the first conductive layer and a second interconnection between a second conductive termination of the embedded component and the second conductive layer.

17. (Original) The substrate assembly of claim 16, wherein the first interconnection is formed through an opening in the first conductive layer and first adhesive layer and the second interconnection is formed through an opening in the second conductive layer and the second adhesive layer.

18. (Original) The substrate assembly of claim 13, wherein at least one among the first conductive layer and the second conductive layer form a conductive pattern on a surface of the substrate assembly.

19. (Original) The substrate assembly of claim 13, wherein the first conductive layer and the second conductive layer are formed from copper and the first adhesive layer and the second adhesive layer are formed from materials selected from the group comprising epoxy resin, epoxies, thermosetting organic materials, PTFEs, thermoforming organic materials, liquid dielectrics, glass reinforced prepregs, thermal plastic dielectrics, and paste dielectrics.

20. (Original) The substrate assembly of claim 13, wherein the substrate core comprises a substrate having a patterned conductive layer on at least one among the bottom surface and the top surface of the substrate core.

21. (Original) The substrate assembly of claim 13, wherein the embedded component is placed within the via in a vertical orientation.

22. (Original) The substrate assembly of claim 13, wherein the embedded component is a component selected from the group comprising a capacitor, a resistor, an inductor, and any combination thereof.

23. (Original) The substrate assembly of claim 14, wherein the interconnection forms a soldering pad for a device mounted on the substrate assembly.

24. (Original) The substrate assembly of claim 23, wherein the device is a ball grid array.

25. (Cancelled) ~~The substrate assembly of claim 13, wherein the first adhesive layer and the second adhesive layer both at least partially fill the via.~~

26. (Original) A method of forming an embedded component in a substrate assembly, comprising the steps of:

applying a first adhesive layer on a first carrier;

placing a pre-processed substrate on the adhesive layer, wherein the pre-processed substrate includes at least a via;

placing the embedded component in the via, wherein the embedded component includes at least two conductive terminations;

applying a second adhesive layer on at least portions of the pre-processed substrate and above at least portions of the embedded component;

placing a second carrier on the second conductive layer; and

biasing the first and second carriers towards each other to create the substrate assembly having the embedded component between the first and second adhesive layers.

27. (Amended) A substrate assembly having at least one embedded component in a via of a substrate core, comprising:

a first adhesive layer coupled to a bottom surface of the substrate core;

an embedded component in the via, wherein the embedded component includes at least two conductive terminations and at least a portion of the first adhesive layer lies below the embedded component; and

a second adhesive layer on at least portions of a top surface of the substrate core and above at least portions of the embedded component, wherein at least one among the first adhesive layer and the second adhesive layer at least partially fills the via.

28. (Original) The substrate assembly of claim 27, wherein the substrate assembly further comprises a first conductive layer adhered to the bottom surface of the substrate core using the first adhesive layer and a second conductive layer on the second adhesive layer.